AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-6 (cancelled)

7. (original) A semiconductor device comprising:

a first memory cell having a first MIS transistor, a second MIS transistor, a third MIS transistor and a fourth MIS transistor, which are of an N channel type;

a second memory cell having a fifth MIS transistor, a sixth MIS transistor, a seventh MIS transistor and an eighth MIS transistor, which are of an N channel type,

wherein the gate-insulating film thickness of said first MIS transistor is smaller than that of said fifth MIS transistor.

8. (original) The semiconductor device according to claim 7, further comprising:

a ninth MIS transistor in an input/output circuit;

a logic circuit having a tenth MIS transistor,

wherein

the gate-insulating film thickness of said ninth MIS transistor is larger than that of said first MIS transistor,

the gate-insulating film thickness of said tenth MIS transistor is smaller than that of said fifth MIS transistor.

9. (original) The semiconductor device according to claim 7, further comprising:

an input/output circuit; and

a logic circuit, wherein

the gate-insulating film thickness of the MIS transistor in said logic circuit is equal to that of said first MIS transistor,

the gate-insulating film thickness of the MIS transistor in said input/output circuit is equal to that of said fifth MIS transistor,

said first memory cell has a ninth MIS transistor and a tenth MIS transistor, which are of a P channel type,

said second memory cell has an eleventh MIS transistor and a twelfth MIS transistor, which are of a P channel type,

the gates of said third MIS transistor and said fourth MIS transistor are connected to a wordline, the gate of

said first MIS transistor is connected to said fourth MIS transistor, the drain thereof is connected to said third MIS transistor, the gate of said second MIS transistor is connected to said third MIS transistor, and the drain thereof is connected to said second MIS transistor,

the gates of said seventh MIS transistor and said eighth MIS transistor are connected to a wordline, the gate of said fifth MIS transistor is connected to said eighth MIS transistor, the drain thereof is connected to said seventh MIS transistor, the gate of said sixth MIS transistor is connected to said seventh MIS transistor, and the drain thereof is connected to said eighth MIS transistor.

10. (original) The semiconductor device according to claim 7, further comprising:

a ninth MIS transistor having a source-drain path between the operating voltage supply point of said first memory cell and the power line,

wherein said ninth MIS transistor is controlled so as to be in the off state in a first state and to be in the on state in a second state,

before said second state is changed to said first state, information of said first memory cell is stored into said second memory cell.

Claims 11-15 (cancelled)